REMARKS/ARGUMENT

Claim 44, objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, has been so amended. Accordingly, Claim 44 is in allowable form.

Examiner objects to the drawings under 37 CFR 1.83(a), for the following reason:

> The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of *"wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter"* must be shown or the features(s) canceled from the claims(s). No new matter should be entered (OA, page 22, lines 9-14).

Applicants respectfully traverse Examiner's above objection. Regarding the limitation, *"wherein the all-digital phase-lock loop is operating in a type-I mode ..."*, Fig 6 shows the ADPLL block diagram. As described in [0042] of the publication, the "type-I mode" is engaged by turning off the integral factor rho in loop filter 215. As a result, Fig. 6 does show this feature.

Regarding the limitation, *"... and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter"*, it is described in [0057] "If the ADPLL is operating in a type-I mode, then an IIR filter can be added to perform the needed filtering of the frequency error." The IIR filter is simply connected to the output of the phase detector 210 or loop filter 215 in Figures 2, 3, 6, 10. Since there is only

scaling and no real frequency filtering in loop filter 215 in type-I, the input or output connection point does not matter. In Fig 10, the IIR filter is realized by processor 1010.

For the reasons set forth above, the objection to the drawings under 37 CFR 1.83(a) is improper and must be withdrawn.

1) Claims 1, 3, 5-8, 11, 13-14, 24-29, 31, 41-43 are stand under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski)(US Publication 2002/019727 A1) in view of Wong et al. (hereinafter Wong)(US Patent 5,295,079). Applicants respectfully traverse this rejection as set forth below.

Claim 1 requires and positively recites, a **method for testing a radio frequency (RF) circuit** comprising: "**observing a signal from the RF circuit**, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating".

In contrast, Staszewski teaches an all-digital phase-locked loop (ADPLL), which contains a digital phase error (PHE) signal. The reference describes an apparatus **but does not teach or even suggest a method of testing it**, as set forth below.

1. "A method for testing a radio frequency (RF) circuit" recited in the preamble is not taught or even suggested in Staszewski.

2. The step of "observing a signal from the RF circuit" is not taught in Staszewski. Due to the lack of testing there, there is no motivation of doing so. The "signal", equated by Examiner to PHE in Fig. 4a is not suggested to be observed for the

purpose of testing. The PHE signal is only fed to the gain circuit 70 as part of a normal ADPLL operation, which has nothing to do with testing. No other connections are shown, especially to the "outside of the RF circuit".

3. The limitation of "wherein the signal has a high degree of correlation with an RF output of the RF circuit" is not taught or suggested in Staszewski. At the time of the reference patent publication, the ADPLL idea was still quite new and it would not have been known by one of average skill in the art that the PHE signal has a high degree of correlation with "an RF output", such as output of the PA circuit.

In addition to the above, Examiner admits that Staszewski fails to teach or suggest, "wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating", as further required by Claim 1. As such, Staszewski fails to teach or suggest, a **method for testing a radio frequency (RF) circuit** comprising: "**observing a signal from the RF circuit**, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and **wherein the observing occurs outside of the RF circuit**", "**manipulating the signal outside of the RF circuit**" and "**producing a metric for the test outside of the RF circuit based on results from the manipulating**", as required by Claim 1.

Applicants respectfully traverse Examiner's new determination that, *"Staszewski does teach observing a signal "PHE" from the RF circuit (See Fig. 4a)(OA, dated 12/26/2008, page 3, lines 2-3).* In reality, the "PHE" signal is not "observed", which implies an outside observer. The PHE signal is merely used as part of a PLL operation, which is entirely an internal environment. There is no "observation" of the PHE signal. Moreover, even if there were, which there is not, Examiner had not identified what it is that is "observing" the PHE signal. Further, the limitation "wherein the observing occurs outside the RF circuit" is not met in Staszewski and Examiner admits this in this

OA (page 24, lines 16 & 17) and previously admitted that this was the case (OA dated 03/26/2008, page 11, lines 17-18).

Examiner, however, relies upon Wong as providing the steps of "wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating", as further required by Claim 1 (Office communication, page 11, lines 17-20). Applicants respectfully respond that even if, arguendo, Wong teaches the above steps identified by Examiner, Wong fails to teach or suggest the previously identified deficiencies of the Staszewski reference. As such, any combination of Staszewski and Wong fails to teach or suggest, "a **method for testing a radio frequency (RF) circuit** comprising: "**observing a signal from the RF circuit**, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating", as further required by Claim 1.

Applicants respectfully traverse Examiner's new determination that, *"one skilled in the art would know that by filtering out frequencies components (not desired) which are above the cut off frequency of the loop filter, a high degree of correlation between the phase error (desired frequencies) and the RF output can be achieved – this is notoriously well known in ADPLLs (OA, page 3, lines 12-16)".* Examiner's determination is not correct. While PLL filtering of external signals is well known, use of PLL filtering for "internal" signals, as required by the limitation "signal from within a processing portion of the RF circuit", is not known. In the event Examiner does not withdraw this determination, Applicants respectfully request that Examiner cite a reference to support this determination.

Applicants further traverse Examiner's new determination that *"examiner did not rely solely in the reference to Staszewski to reject claim 1 – the examiner used the combination of Staszewski and Wong to reject claim 1 (OA, page 4, lines 2-4)"*. Applicants respectfully point out that in Wong, the system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output – making them available (despite various technical difficulties) would not provide any substantial benefits. As such, Examiner's determination is supposition not supported by fact – little more than improper hindsight reconstruction.

For the reasons set forth above, Wong, alone or in combination with Staszewski, does not teach or suggest "**a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals**", as required by Claim 1. The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed. For the reasons set forth above, the 35 U.S.C. 103(a) rejection of Claim 1 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claim 1, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only**

by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification**. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious**. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claim 41 requires and positively recites, a circuit comprising: "a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase", "a phase detector coupled to the reference phase accumulator, the **phase detector containing circuitry to compute a difference between the reference phase and a variable phase**", "a digitally-controlled oscillator (DCO) coupled to the phase detector, **wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation**" and "a variable phase accumulator coupled to the DCO and the phase detector, **the variable phase accumulator containing circuitry to compute the variable phase**".

Staszewski does not teach "**wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation**" limitation, as required by Claim 41. It is not obvious, and Examiner has provided no evidence to the contrary, how one having ordinary skill in the art at the time of the invention would apply teachings in Wong to test the DCO.

To copy from the previous amendment: <<Claim 41 requires, "the phase detector containing circuitry to compute a difference between the reference phase and a variable phase ....". Wong only teaches UP/DOWN phase direction information, which is not the phase error estimation signal. There is no magnitude information, only the direction.">>. As such, Examiner's determination of the teaching of Wong is erroneous.

Applicants traverse Examiner's new determination that, *"the reference of Wong does teach that the signal is the phase error – (See fig. 2 & col. 2, lines 50-57 "phase error information"*. Applicants respectfully reply that at best, Wong's signal is only the magnitude of the phase error.

In light of the above, any combination of Staszewski and Wong fails to teach or suggest, "**wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation**" limitation, as required by Claim 41. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 41 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claim 41, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claims 3, 5-8, 11, 13-14, 24-29, 31, 42 and 43 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 3 further defines the method of claim 1, **wherein the signal is a phase error signal**. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 5 further defines the method of claim 3, wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest. Claim 5 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Moreover, Applicants disagree with Examiner's contention that one skilled in the art "would know that if the loop filter is designed in such as way (adjusting filter's parameters) so that the frequency of the error signal is within the cutoff frequency of the loop filter, then a high degree of correlation can be achieved between the error signal and the output signal". Applicants respectfully request Examiner to provide evidence from the prior art supporting his assertion or withdraw the determination. Furthermore, when a high degree of correlation is achieved the transfer function will be flat within a specific frequency range". At the time of the instant application, the knowledge that the digital PHE signal was highly correlated with the RF output phase, and their transfer function was flat, was not obvious.

Claim 6 further defines the method of claim 1, wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. Claim 6 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 7 further defines the method of claim 6, wherein the signal is an output of a phase detector. Claim 7 is allowable for the same reasons set forth above in support of the allowance of Claim 6.

Claim 8 further defines the method of claim 7, wherein the signal has been filtered. Claim 8 is allowable for the same reasons set forth above in support of the allowance of Claim 7. Moreover, Examiner's interpretation of Wong is simply incorrect. First, the circuit disclosed in Wong's Fig. 2 is not an "all digital circuit" (as required by the parent Claim 6), but rather a "very high frequency phase locked loop" with a number of analog components and signals. The Digital Loop Filter 14 in Wong does not operate on a digital phase error signal but analog UP/DOWN pulses in which the information is contained in the pulse widths. The analog nature of circuit 14 is described in col. 3 as "The loop filter 14 of the DPLL includes a scaler circuit, an integrator circuit, and a summing circuit emulating a 1-pole/1-zero digital loop filter".

Applicants respectfully traverse Examiner's new determination that, *"the reference to Wong does teach that the PLL is a Digital Phase Lock Loop (see col. 3, line 14, col. 4, lines 36-37 "DPLL" (OA, page 9, lines 5-6)"*. Applicants respectfully point out that Examiner's determination is a commonly known misnomer. DPLL is an improvement over analog PLL. At that time (decades ago) it was considered a great progress when adding a single logic gate would somehow make it digital. However, it is still analog intensive. Hence the new term all-digital PLL (ADPLL) that claims the fully digital nature of PLL. Note the claim limitation is not "digital PLL" but "all-digital PLL", as well as "all-digital circuit". As a result, Examiner's combination of Staszewski and Wong to obviate Claim 8 is improper and must be withdrawn.

Claim 11 further defines the method of claim 8, wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output

of the loop filter. Claim 11 is allowable for the same reasons set forth above in support of the allowance of Claim 8.

Claim 13 further defines the method of claim 1, wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. Claim 13 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 14 further defines the method of claim 1, wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal. Claim 14 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Morevoer, Examiner is incorrect in determining that Wong teaches "test ... for phase error trajectory". "Phase error trajectory" requires transmit modulation and the circuit in Wong is not capable of dealing with it.

Claim 24 further defines the method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. Claim 24 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, the text in Wong cited by Examiner does not teach "the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth", as required by Claim 24. The text only mentions setting of various programmability modes, NOT bandwidths: "The loop filter also includes a loop configuration circuit which in response to the digital tester 4 programs and via the LCP 24 configures the loop type of the DUT 2. The DPLL, for example, provides for eight different types of loop configurations in a test mode (8 different combinations of close loop, open loop, and enable/disable proportional/integral paths) as shown in Table 1."

Applicants respectfully traverse Examiner's determination that, *"Wong does teach "the loop filter also includes a loop configuration circuit for configuring the loop type of the DUT (see col. 3, lines 19-25 & table 1)(OA, page 9, line 21 – page 10, line 1)".* Applicants respectfully respond that "loop type" is not a proper way of "setting the all-digital phase-locked loop to a certain bandwidth". Changing of loop type only introduces a pole at origin and does not control its bandwidth. At best, its effect would be parasitic or useless for a practical application. For the reasons set forth above, any combination of Staszewski and Wong fails to teach or suggest all of the elements of Claim 24. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Applicants further traverse citation to Girardeau and Yamaguchi regarding Claim 24. The combination of these two references is not currently cited against Claim 24. Accordingly, the citation to Girardeau and Yamaguchi must be withdrawn.

Claim 25 further defines the method of claim 24, wherein the test is for estimating phase noise power and the signal is an output of a phase detector, and wherein the manipulating comprises calculating a mean square error of the signal. Claim 25 is allowable for the same reasons set forth above in support of the allowance of Claim 24. Moreover, the text identified by Examiner about recovered clock (RXC) jitter is irrelevant. It requires applying a "preconditioned input data pattern at the DPLL input (Din input on FIG. 2)", which is not applicable in the present invention. The present invention pertains to an ADPLL and a transmitter and does not concerns itself with the recovered clock. As such, any combination of Staszewski and Wong fails to teach or suggest all of the elements of Claim 25. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 26 further defines the method of claim 25, wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop

bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths. Claim 26 is allowable for the same reasons set forth above in support of the allowance of Claim 25. Moreover, Wong does not teach selecting different loop bandwidths. The loop configuration in the cited text selects, for example, between open loop, closed loop, etc, modes, which have nothing to do with selecting loop bandwidths. As such, Wong does not teach their repeated application of "setting, observing, and manipulating" "for several different all-digital phase-locked loop bandwidths", as required by Claim 26. The statement by Examiner "Furthermore, one skilled in the art would know that the loop bandwidth varies depending if the PLL is in either acquisition or tracking mode" attempts to suggest obviousness but is irrelevant here since the loop bandwidth change in the present invention has nothing to do with PLL acquisition or tracking mode, but pertains to the testing method itself.

Applicants respectfully traverse Examiner's new determination that, *"the loop bandwidth is dependent on what type of loop configuration the PLL will be operating (OA, page 11, lines 2-3)"*. In reality, loop type (I or II) cannot be reliably used as a means to control "several different all-digital phase-lock loop bandwidths". For the reasons set forth above, any combination of Staszewski and Wong fails to teach or suggest all of the elements of Claim 26. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 27 further defines the method of claim 1, wherein the RF circuit is an all-digital frequency synthesizer. Claim 27 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 28 further defines the method of claim 1, wherein the RF circuit is an all-digital transmitter. Claim 28 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 29 further defines the method of claim 28, wherein the transmitter is used in a wireless communications network. Claim 29 is allowable for the same reasons set forth above in support of the allowance of Claim 28.

Claim 31 further defines the method of claim 1, wherein the testing comprises a functional test or a compliance test of the RF circuit. Claim 31 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Applicants further traverse citation to Girardeau and Yamaguchi regarding Claim 24. The combination of these two references is not currently cited against Claim 24. Accordingly, the citation to Girardeau and Yamaguchi must be withdrawn.

Claim 42 further defines the circuit of claim 41 further comprising a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock. Claim 42 is allowable for the same reasons set forth above in support of the allowance of Claim 41.

Claim 43 further defines the circuit of claim 41 further comprising a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase. Claim 43 is allowable for the same reasons set forth above in support of the allowance of Claim 41.

2) Claims 15-17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski)(US Publication 2002/019727 A1) in view of Wong et al. (hereinafter Wong)(US Patent 5,295,079), as applied to claim 1 above, and further in view of Girardeau. Applicants respectfully traverse this rejection as set forth below.

Claim 15 further defines the method of claim 14, wherein the phase error trajectory is good when the change in the signal is less than a specified threshold. Claim 15 is allowable for the same reasons set forth above in support of the allowance of Claim 14. Moreover, none of the references pertain to the "test ... for phase error trajectory". Further, the references, alone or in combination, do not teach the limitation of "wherein the manipulation comprises measuring a change in the signal". Examiner's statement, "The error signal is further compared with a threshold in order to determine if a coarse or fine adjustment is needed", is irrelevant as it does not pertain to "change in the signal" and testing in general.

Applicants further traverse Examiner's new determination that, "one skilled in the art would know that the phase error is the main signal of interest within a PLL (OA, page 11, lines 15-16)". Applicants respectfully submit that Examiner confuses "phase error trajectory" with "phase error". The two are different. Accordingly, for the reasons set forth above, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 15. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 16 further defines the method of claim 14, wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. Claim 16 is allowable for the same reasons set forth above in support of the allowance of Claim 14. Moreover, none of the references teach or suggest "measuring a

peak, a variance, or a rate of change in the signal". The circuits are not designed for and are not capable of these measurements. The Examiner's cited text "Preferably, an error signal 104 compares unfavorably when it exceeds the coarse threshold -- when the coarse threshold signal is logic high" (col. 5, lines 37-39) has noting to do with the limitation of "comparing a value of the signal over several samples".

Applicants further traverse Examiner's new determination that, "the error signal is compared to a threshold in order to determine if synchronization is achieved and/or maintained – this is notoriously well known in PLLs (OA, page 12, lines 8-10)". Applicants respectfully submit that Examiner again confuses "phase error trajectory" with "phase error". The two are different. Accordingly, for the reasons set forth above, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 16. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 17 further defines the method of claim 1, wherein the test is for frequency lock and the signal is the output of a phase detector, and wherein the manipulation comprises comparing a value of the signal over several samples. Claim 17 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, Examiner's cited text "Preferably, an error signal 104 compares unfavorably when it exceeds the coarse threshold -- when the coarse threshold signal is logic high" (col. 5, lines 37-39) has noting to do with the above limitation. As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 17. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 19 further defines the method of claim 17, wherein the samples are taken at different times. Claim 19 is allowable for the same reasons set forth above in support of the allowance of Claim 17. Moreover, Examiner's cited text "Preferably, an error

signal 104 compares unfavorably when it exceeds the coarse threshold -- when the coarse threshold signal is logic high" (col. 5, lines 37-39) has noting to do with the above limitation. Further, and contrary to Examiner's determination, Girardeau does NOT teach the limitation of "wherein the samples are taken at different times". As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 19. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 20 further defines the method of claim 1, wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter, and wherein the manipulation comprises comparing the signal with a specified range. Claim 20 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, the references, alone or in combination, do not teach the limitation of "wherein ... the signal is an output of an integral accumulator of a loop filter". The text cited by Examiner "The DPLL 10 determines a correct divisor upon startup, corrects for frequency drifts, 20 and is able to operate in noisy conditions" (col. 5, lines 19-21) is irrelevant and does not mention the "integral accumulator of the loop filter". Furthermore, the references fail to teach "wherein the manipulation comprises comparing the signal with a specified range". Comparing with a threshold is not equivalent with comparing with a specified range. In the event Examiner maintains this argument, Applicants respectfully request that Examiner provide evidence from the prior art supporting his determination. As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 20. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

Claim 21 further defines the method of claim 20, wherein the frequency deviation is within acceptable limits when the signal is within the specified range.

Claim 21 is allowable for the same reasons set forth above in support of the allowance of Claim 20.

Examiner sets forth a rejection for Claim 22, but it is not reflected in his listing of Claims rejected on page 20, line 1 of the Office communication of March 26, 2008. Accordingly, Applicants do not know if Claim 22 is rejected or not. Examiner must clarify whether or not Claim 22 is rejected. Nevertheless, for the purposes of this amendment, Applicants will assume it is rejected under the same grounds set forth on page 20, line 1 of the Office communication of March 26, 2008.

Claim 22 further defines the method of claim 20, wherein the manipulation further comprises comparing several samples of the signal. Claim 22 is allowable for the same reasons set forth above in support of the allowance of Claim 20. Moreover, the references fail to teach the limitation of "comparing several samples of the signal". The text cited by the Examiner does not mention it. As such, any combination of Staszewski, Wong and Girardeau fails to teach or suggest all of the elements of Claim 22. The 35 U.S.C. 103(a) rejection is erroneous and must be withdrawn.

3) Claim 45 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claims 1 and 41 above, and further in view of Ko et al. (US 5,982,832). Applicants respectfully traverse this rejection as set forth below.

Claim 45 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion. Claim 45 is allowable for the same reasons set forth above in support of the

allowance of Claim 44. Moreover, Figure 4 in Ko does not show "a plurality of filters arranged in a parallel fashion", as suggested by Examiner. The cited text (col. 2, lines 45-52) describes the structure filters as n filters with the phase detector selecting one filter among the n filters. In addition, combining Ko into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23. As such, any combination of Girardeau, Yamaguchi and Ko fails to teach or suggest all of the elements of Claim 45. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

4) Claim 46 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claims 1 and 41 above, and further in view of Cucchietti et al. (US 4,819,080). Applicants respectfully traverse this rejection as set forth below.

Claim 46 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. Claim 46 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Moreover, Combining Cucchiett into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

5) Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claim 1 above, and further in view of Kim et al. (US 6,885,700). Applicants respectfully traverse this rejection as set forth below.

Claim 2 further defines the method of claim 1, wherein the testing is performed using built-in self test (BIST) techniques. Claim 2 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Furthermore, the combination of Girardeau, Yamaguchi and Kim does not satisfy the limitation "wherein the **testing** is performed", which is positively recited and required by Claim 2. Girardeau does not teach or even suggest testing and incorporating Yamaguchi and Kim will change nothing in this regard.

Kim's teaching of BIST is not applicable to the combination of Staszewski and Wong. Kim teaches the use of the traditional pulse-based phase detector and charge pump. It also requires the VCO divider. None of these circuits is used in Staszewski so Kim is not relevant here.

Moreover, combining Kim into Girardeau does not make sense because the objective of the DPLL in Girardeau is not test or even built-in self-test (BIST) but the main or mission mode of its operation, which includes agility and being robust over the changing environment. Girardeau teaches an apparatus and method for determining a feedback divider ratio in a digital phase locked loop (DPLL) by monitoring the drift in the feedback signal. The drift could be caused by using an unknown frequency of fixed frequency system clock 22. (col. 2, lines 28-39). Hence monitoring the frequency drift of the external clock is not related to testing, so there is no motivation to incorporate Kim. Furthermore, the test or BIST would imply reporting back the results outside of the circuit. No such mechanism is reported in Girardeau simply because he does not teach the test or BIST. As such, any combination of Staszewski, Wong and Ko fails to teach or suggest all of the elements of Claim 2. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

6) Claims 9, 12, 30 & 47 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski)(US Publication 2002/019727 A1), and Wong et al. (hereinafter Wong)(US Patent 5,295,079), as applied to claim 1 above, and further in view of Staszewski et al. (hereinafter Staszewski 1)(US Publication 2002/0094052). Applicants respectfully traverse this rejection as set forth below.

Claim 9 further defines the method of claim 8, wherein the all-digital phase-lock loop is operating in a type-II mode, and the signal is an output of an integral accumulator of a loop filter. Claim 9 is allowable for the same reasons set forth above in support of the allowance of Claim 8. Moreover, the references alone, or in combination, fail to teach that the "signal" is an output of an integral accumulator. The text relied upon by Examiner does not support Examiner's determination: "The loop filter 14 of the DPLL includes a scaler circuit, an integrator circuit and a summing circuit emulating a 1-pole/1-zero digital loop filter." It mentions three blocks, only one of which is the integrator. As such, any combination of Staszewski, Wong and Staszewski 1 fails to teach or suggest all of the elements of Claim 9. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 12 further defines the method of claim 6, wherein the signal is an output of a gain normalization block. Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 6. Moreover, there is no teaching or suggestion in Staszewski that the "output of a DCO gain normalization block" can be used to testing purposes. In the event Examiner maintains this rejection Applicants request Examiner to specifically point out such teaching in the Staszewski reference. As such, any combination of Staszewski, Wong and Staszewski 1 fails to teach or suggest all of the elements of Claim 12. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 30 further defines the method of claim 29, wherein the wireless communications network is Bluetooth compliant. Claim 30 is allowable for the same reasons set forth above in support of the allowance of Claim 29.

Claim 47 further defines the circuit of claim 41 further comprising a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. Claim 47 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Moreover, there is no teaching or suggestion in Staszewski that the "output of a DCO gain normalization block" can be used to testing purposes. In the event Examiner maintains this rejection Applicants request Examiner to specifically point out such teaching in the Staszewski reference. As such, any combination of Staszewski, Wong and Staszewski 1 fails to teach or suggest all of the elements of Claim 47. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

7) Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski)(US Publication 2002/019727 A1), and Wong et al. (hereinafter Wong)(US Patent 5,295,079), as applied to claim 1 above, and further in view of Gustafson et al (hereinafter Gustafson)(US Patent 4,086,539). Applicants respectfully traverse this rejection as set forth below.

Claim 18 further defines the method of claim 17, wherein the frequency has been locked when a variance in the magnitude is less than a specified threshold. Claim 18 is allowable for the same reasons set forth above in support of the allowance of Claim 17. Further, regarding the text in Gustafson relied upon by Examiner: "The

phase-lock loops discussed in the article are of classical design and they produce very favorable results in terms of phase-error variance in high frequency systems and below threshold". The text below the excerpt cited by Examiner defines the term "below threshold" as entirely different from the definition in the instant application: <The term "below threshold" 40 denotes the region where the nonlinearity in the classical PLL is essentially linear (i.e. the sine of the error in the estimate of phase is approximately equal to the error in the estimate of phase).> (col. 1, lines 40-43). This makes it irrelevant. As such, any combination of Staszewski, Wong and Gustafson fails to teach or suggest all of the elements of Claim 18. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

8) Claims 32-40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 5,295,079). Applicants respectfully traverse this rejection as set forth below.

Independent Claim 32 requires and positively recites, a circuit comprising: "a processor coupled to a radio frequency (RF) circuit, the processor containing circuitry to manipulate digital signals from the RF circuit **to provide a performance metric for the RF circuit**" and "**a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals**".

In contrast, Wong describes a phase locked loop (PLL) nominally operating at 125 MHz for clock recovery of a 125 Mbits/s FDDI data. The PLL contains access ports connected to an I/O controller that interfaces with an external Tester 4. The PLL consists of a Phase Detector 10, Phase Error Processor (PEP) 12 performing phase error

decimation and quantization and outputting 1-bit digital signal carrying UP/DOWN and Data_valid flag, Loop Filter 14 controlled by Loop Configuration Port (LCP) 24, Phase-to-Frequency Converter (PFC) 16 to generate a triangular wave of controllable frequency, and a Frequency Controlled Oscillator (FCO) 18. The FCO operates at two times the output frequency and is fed by equally-spaced 250 MHz clock and is followed by a divide-by-two 20 circuit. The loop filter integral signal couples with Frequency Access Port (FAP) 26. The accumulated ("sawtooth patterns") up/down bits are coupled with the Phase Access Port (PAP) 28. The PEP outputs are decimated by 44, so its output data rate as well as any other 'down-stream' circuit until the FCO is 125Mbps/44=2.84Mbps. The I/O controller link 6 connects the tester 4 with the LCP 24, FAP 26 and PAP 28.

Wong's system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output – making them available (despite various technical difficulties) would not provide any substantial benefits. For the above reasons, Wong does not teach or suggest, "**a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.**" The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed, as suggested by Examiner.

Moreover, Wong does not teach or suggest the limitation of "to provide a performance metric for the RF circuit", as further required by Claim 32. Wong teaches only testing and does not even suggest performance estimation. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claims 33-40 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 33 further defines the circuit of claim 32 further comprising a latch coupled to the processor, the latch to store the performance metric provided by the processor.

Claim 34 further defines the circuit of claim 32, wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. Claim 34 is allowable for the same reasons set forth above in support of the allowance of Claim 32.

Claim 35 further defines the circuit of claim 34, wherein the first and the second integrated circuits are the same integrated circuit. Claim 35 is allowable for the same reasons set forth above in support of the allowance of Claim 34.

Claim 36 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. Claim 36 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Furthermore, Examiner is not correct in asserting that the processor in Wong "is coupled to an output of a phase detector". The tester 4, equated by Examiner to the processor, is coupled only to LCP, FAP and PAP, with FAP being the closest to the output of the phase detector. The phase detector 10 output contains information of the phase error, which is the phase difference between the Din and P_CLK inputs to the phase detector. FAP 26 register, on the other hand, contains "the frequency difference between Din and the local clock generated by the local crystal" (col. 4, lines 60-62) – this is definitely not the phase error. Hence, the tester 4 is not coupled to the phase detector. Moreover, Won does not teach either an all-digital phase

locked loop or coupling the processor to an output of a phase detector. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 37 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector. Claim 37 is allowable for the same reasons set forth above in support of the allowance of Claim 32.

Claim 38 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. Claim 38 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Furthermore, Examiner is not correct in asserting that the processor in Wong "is coupled to an output of a phase detector". The tester 4, equated by Examiner to the processor, is coupled only to LCP, FAP and PAP, with FAP being the closest to the output of the phase detector. The phase detector 10 output contains information of the phase error, which is the phase difference between the Din and P_CLK inputs to the phase detector. FAP 26 register, on the other hand, contains "the frequency difference between Din and the local clock generated by the local crystal" (col. 4, lines 60-62) – this is definitely not the phase error. Hence, the tester 4 is not coupled to the phase detector. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 39 further defines the circuit of claim 32, wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. Claim 39 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Moreover, Wong does not teach all four aspects of testing: "testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field", as required by Claim 39. The text cited by Examiner discusses only a "cost efficient

comprehensive testing" at IC level and communication board level. It mentions "in field servicing (on-site)", which simply implies a lab environment and is different from "in field" testing. The specification of the instant application describes ([0048] of the publication) "in field testing" as "testing can usually be done without the use of expensive laboratory equipment", and "the testing can be performed while the electronic device is in the end-user's hands". The system in Wong with the external test equipment 4 in Fig. 2 is simply not capable of "in-field testing". Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 40 further defines the circuit of claim 32, wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a phase noise power, or combinations thereof. Claim 40 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Further, as stated already in other places, Wong does not teach or suggests testing of "phase trajectory error" since there is no frequency modulation capability. Similarly, Wong does not teach or suggests testing of "phase noise power". Measuring of a peak jitter does not help with estimating the phase noise power. The instant application describes a method for estimating the phase noise power in paragraph [0058] and in Figure 9d. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

9) Claims 48-50 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim)(US Patent 6,885,700 B1) in view of Ortiz Perez et al (hereinafter Perez)(US Patent 5,966,428). Applicants respectfully traverse this rejection as set forth below.

Claim 48 requires and positively recites, a method for operating a cellular phone, comprising: "**performing built-in self-test (BIST) on a parameter associated with the cellular phone**" and "reporting to a cellular service provider through a wireless medium when the BIST reports the parameter to be degraded beyond a limit".

Examiner admits that Kim fails to teach or suggest, "reporting to a cellular service provider through a wireless medium when the BIST reports the parameter to be degraded beyond a limit" (Office communication page 31, lines 3-5). Examiner relies instead on Perez to provide this teaching. But even if, arguendo, Perez provides this teaching, Examiner misinterprets the remaining teaching of Kim. In actuality, Kim describes fault testing of a PLL, which is a narrow area well defined in the arts. To cite from Kim: "structural and defect-oriented testing" (Abstract), "defect-oriented testing" (col. 2, line 10). It does not teach performance testing associated with a cellular phone, nor does it even go beyond the PLL, which is merely a small building block of a cell phone. Specifically he does not teach "performing built-in self-test (BIST) on a parameter associated with the cellular phone", as required by Claim 48.

Therefore, even if, arguendo, Perez teaches what Examiner proposes, the combination of Kim and Perez yet fails to teach or suggest, "**performing built-in self-test (BIST) on a parameter associated with the cellular phone**", as required by Claim 48.

Applicants traverse Examiner's new determination that, *"the combination of Kim and Perez does suggest the teaching of performing built-in self-test (BIST on a parameter associated with the cellular phone – (In Perez, see abstract, col. 5, line 26 – col. 6, line 15)(OA, page 20, lines 15-18)"*. At best, Perez teaches basic fault testing, but NOT "**built-in self-test (BIST) on a parameter associated with the cellular**

phone", as required by Claim 48. Accordingly, for the reasons set forth above, the 35 U.S.C. 103(a) rejection of Claim 48 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claim 48, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claims 49, 50 and 52-54 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 49 further defines the method of claim 48, wherein the performing step is done on power-up of the cellular phone. Claim 49 is allowable for the same reasons set forth above in support of the allowance of Claim 48.

Claim 50 further defines the method of claim 48, wherein the parameter is an RF system parameter. Claim 50 is allowable for the same reasons set forth above in support of the allowance of Claim 48. Moreover, Wong does not teach "wherein the parameter is an RF system parameter" (as required by Claim 50) "associated with the cellular phone" (as required by the parent Claim 48). As argued above, Kim teaches only a fault testing of a PLL, which is different from an RF system parameter of a cellular phone.

Claim 52 further defines the method of claim 48, further comprising a step of notifying a user of the cellular phone that the parameter is degraded beyond a limit. Claim 52 is allowable for the same reasons set forth above in support of the allowance of Claim 48. Moreover, Perez does not teach reporting the results to the user. Perez only describes reporting the results to an off-site monitoring center.

Claim 53 further defines the method of claim 52, wherein the notifying step is done wirelessly. Claim 53 is allowable for the same reasons set forth above in support of the allowance of Claim 52.

Claim 54 further defines the method of claim 52, wherein the notifying step is done through a service bill. Claim 52 stands allowable for the same reasons set forth above in support of the allowance of Claim 52.

10) Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (hereinafter Kim)(US Patent 6,885,700 B1) and Ortiz Perez et al (hereinafter Perez)(US Patent 5,966,428), as applied to claim 48 above, and further in view of Reddy et al. (hereinafter Reddy)(US Patent 6,636,979 B1). Applicants respectfully traverse this rejection as set forth below.

Claim 51 further defines the method of claim 50, wherein the RF system parameter is a distortion in a phase error trajectory. Claim 51 stands allowable for the same reasons set forth above. Moreover, Reddy does not teach "phase error trajectory" of a data transmission, as suggested by Examiner. Reddy merely describes "measuring phase error between two clocks", which is different. For example, Fig. 5 configuration in Reddy uses a PLL to synthesize a single frequency carrier. The modulation is not taught. As such, any combination of Kim, Perez and Reddy fails to teach or suggest all of the elements of Claim 54. The, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

11) Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Staszewski et al. (hereinafter Staszewski) in view of Yamaguchi et al. (hereinafter Yamaguchi)(US Patent 6,687,629 B1). Applicants respectfully traverse this rejection as set forth below.

Claim 1 requires and positively recites, a **method for testing a radio frequency (RF) circuit** comprising: "**observing a signal from the RF circuit**, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the

RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating".

In contrast, Staszewski teaches an all-digital phase-locked loop (ADPLL), which contains a digital phase error (PHE) signal. The reference describes an apparatus **but does not teach or even suggest a method of testing it**, as set forth below.

4. "A method for testing a radio frequency (RF) circuit" recited in the preamble is not taught or even suggested in Staszewski.

5. The step of "observing a signal from the RF circuit" is not taught in Staszewski. Due to the lack of testing there, there is no motivation of doing so. The "signal", equated by Examiner to PHE in Fig. 4a is not suggested to be observed for the purpose of testing. The PHE signal is only fed to the gain circuit 70 as part of a normal ADPLL operation, which has nothing to do with testing. No other connections are shown, especially to the "outside of the RF circuit".

6. The limitation of "wherein the signal has a high degree of correlation with an RF output of the RF circuit" is not taught or suggested in Staszewski. At the time of the reference patent publication, the ADPLL idea was still quite new and it would not have been known by one of average skill in the art that the PHE signal has a high degree of correlation with "an RF output", such as output of the PA circuit.

In addition to the above, Examiner admits that Staszewski fails to teach or suggest, "wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating", as further required by Claim 1. As such, Staszewski fails to teach or suggest, a **method for testing a radio frequency (RF) circuit** comprising: "**observing a signal from the RF circuit**, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and **wherein the observing occurs outside of the RF circuit**", "**manipulating the signal outside of the**

RF circuit" and "**producing a metric for the test outside of the RF circuit based on results from the manipulating**", as required by Claim 1.

Examiner, however, relies upon Yamaguchi as teaching, "wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit AND producing a metric for the test outside of the RF circuit based on results from the manipulating". As argued previously, Staszewski does not disclose a "method for testing" nor "observing a signal from the RF circuit". Also, the knowledge of the PHE signal being enough correlated with the RF output was not available at the time of invention. Moreover, Yamaguchi does not teach observing a "digital signal", such as PHE of the present invention, much less "manipulating". One cannot connect a spectrum analyzer to a digital or multi-bit signal. Therefore, it is not possible to combine Yamaguchi with Staszewski – this would not work at all! Accordingly, the 35 U.S.C. 103(a) rejection of Claim 1 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claim 1, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed.

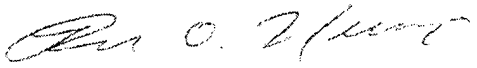
Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

An amendment after a final rejection should be entered when it will place the case either in condition for allowance or in better form for appeal. 37 C.F.R. 1.116; MPEP 714.12. This amendment places the case in condition for allowance. At a minimum the amendment should be entered because it places the case in better form for appeal by reducing the number of claims/issues on appeal.

Claims 1-3 and 5-54 stand allowable over the cited art for the reasons set forth above. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418